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10/716,791	11/19/2003	Hiroaki Kubo	JP920020167US1	6146

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,791	KUBO ET AL.	
	Examiner	Art Unit	
	David N. Werner	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action for US patent application 10/716,791 is in response to the amendment filed 01 October 2007, in reply to the Non-Final rejection of 30 April 2007. Currently, claims 1-7 are pending.

2. In the previous Office action, claim 7 was rejected under 35 U.S.C. 101 as non-statutory, claims 1, 6, and 7 were rejected under 35 U.S.C. 103(a) as obvious over US Patent 6,233,253 B1 (Settle et al.) in view of US Patent 6,297,794 B1 (Tsubouchi et al.), claim 2 was rejected under 35 U.S.C. as obvious over Settle et al. in view of Tsubouchi et al. and in view of US Patent 5,812,760 A (Mendenhall et al.), and claims 3-5 were rejected under 35 U.S.C. 103(a) as obvious over Settle et al. in view of Tsubouchi et al., in view of Mendenhall et al., and in further view of US Patent 5,671,260 A (Yamauchi et al.). In addition, the drawings and disclosure were objected to for informalities.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 26 November 2002. It is noted, however, that applicant has not filed a certified copy of the 2002-342268 application as required by 35 U.S.C. 119(b).

Drawings

4. Replacement drawings were received on 01 October 2007. These drawings are acceptable.

Response to Amendment

5. Applicant's amendments to the specification have been fully considered. The objection to the specification is withdrawn.

6. Applicant's amendment to claim 7 has been fully considered. The rejection of claim 7 under 35 U.S.C. 101 is withdrawn.

Response to Arguments

7. Applicant's arguments filed 01 October 2007 have been fully considered but they are not persuasive. Applicant makes four principal arguments: first, that the cited Settle and Tsubouchi references, when combined, do not teach the claimed feature of "selection of a predetermined amount of video data during an interval between successively detected synchronizing signals", second, that there is no motivation to combine the Settle and Tsubouchi references, third, that the Mendenhall reference does not teach the material of claim 2, and fourth, that the Yamauchi reference does not teach the material of claim 5.

8. In response to Applicant's argument that the prior art cited does not teach "selection of a predetermined amount of said memory as a payload responsive to the packet header", it is respectfully submitted that in Settle et al., "Unit 18b adds MPEG

transport headers and forms MPEG transport packets with the data produced by unit 14 to form MPEG compatible packets" (column 4: lines 39-42). An MPEG-2 transport stream packet always has a length of 188 bytes, with the payload size adjusting based on header length. See, for example, Watkinson, *MPEG*, pp. 357-358, "Transport stream packets are always 188 bytes long". The 188 byte transport stream packet produced by Settle corresponds with the "predetermined amount of video data" contested by Applicant.

9. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as stated in page 5 of the 30 April Office Action, releasing video data stored in a buffer (here, as taught by Settle, the amount of data needed to fill a 188-byte transport stream packet), in response to a synchronizing signal, as taught by Tsubouchi et al., would ensure that video would only be transferred from one of multiple input sources at a time using a single bus, preventing data collision (column 2: lines 43-51). Settle et al. teaches multiplexing data from multiple input sources, such as a satellite feed and a videocassette recorder (column 4: lines 31-34). One of ordinary skill in the art would

have been motivated to look to Tsubouchi et al. at the time the invention was made for assistance in multiplexing.

10. In response to Applicant's argument regarding claim 2, Settle et al. produces as output MPEG transport packets, which are known to have a fixed length of 188 bytes, which must come from the concatenation of a packet header and a packet payload, it is implicit that there are means to determine packet header length and packet length within the MPEG packetizers of Settle et al. to produce valid transport packets. Since Mendenhall does not teach outputting packets of a fixed length, but rather of variable length, Mendenhall is no longer relied on as a reference for claim 2.

11. In response to Applicant's argument regarding claim 5, it is respectfully submitted that a "release" of memory, such as that described in Yamauchi et al. (column 8: line 14) is generally considered by those skilled in the art to be an erasure of that memory. Notice that in Yamauchi et al., the storage and release of memory are controlled by clock signal Sc1, but the reading out of memory is controlled by a second clock signal Sc2 (column 8: lines 28-30), so there should be no confusion between a memory "release", in which no-longer needed memory is made available for new data input, and a memory "read", in which the contents of the memory are accessed and output.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1, 2, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,233,253 B1 (Settle et al.) in view of US Patent 6,297,794 B1 (Tsubouchi et al.), of which corresponding Japanese Patent Application Publication 10-116,064 A was cited in the Information Disclosure Statement of 01 March 2007. Claims 1, 6, and 7 of the present invention are co-extensive in scope with claim 1 as a hardware embodiment, claim 6 as a method, and claim 7 as a software embodiment.

Settle et al. teaches a format conversion system that multiplexes video data from multiple sources into one data format for transmission (abstract). Regarding the "header generation device" of apparatus claim 1, packetizers 18 in Settle et al. add MPEG transport headers to the data from the video sources (column 4: lines 47-49). Regarding the step of "generating a packet header" in method claim 6, the packetizers perform formatting steps 214 and 245, which add packet headers to video data in the method shown in figure 1 of Settle et al. (column 3: lines 23-29, 50-52). Regarding the step of "generating the packet header" in software claim 7, the packetizing method may be implemented on a computer (column 4: lines 26-30). Regarding the "selection of a predetermined amount of video data of said memory as a payload responsive to the packet header" in claims 1, 6, and 7, Settle et al. produces MPEG-2 transport stream packets (column 4: lines 39-42), which were known to have a fixed length of 188 bytes each, comprising the packet header and packet payload data.

Although in the header-generating device of Settle et al. clock references are periodically added to a resultant multiplexed transport stream (column 5: lines 63-66), this information is used to synchronize audio and video data at a decoding step, not at encoding, and so does not correspond with the claimed "synchronizing signal".

Tsubouchi et al. teaches a system with a variety of video devices, including a video capture device (column 8: lines 17-25) and MPEG encoder (column 6: lines 50-58), which share a dedicated bus for audio/video data. Each device includes an output buffer for outputting data onto the bus (column 2: lines 55-57). This bus includes a ZV control line, on which an enable signal can be transmitted. The control line may be daisy-chained to each device (column 5: lines 27-36), or it may be common to all devices (column 10: lines 13-15). In one embodiment, a pulse generating circuit in each device sends out a pulse on the control line to disable other devices and free up the A/V bus for data transmission (column 11: lines 32-58). Then, the enable signal corresponds with the claimed "synchronizing signal". The setup is pulse-width modulated, with each pulse generating circuit producing a pulse of a different width (column 11: lines 10-32). Each device also includes a flip-flop that stores the enable/disable state for the device. A particular device can only use the video when its flip-flop is set to enable (column 10: lines 41-56). Then, until a pulse from a different device is detected, resetting the flip-flop, a device may be free to output video to the bus. Then, these flip-flops correspond with the claimed “synchronous timing detector” in claim 1, and the resetting of a flip-flop corresponds with the claimed “detecting a synchronization signal”.

Settle et al. discloses the claimed invention except for generating packetized video in response to a synchronization signal. Tsubouchi et al. teaches that it was known to store video in a buffer, and only read out from the buffer in response to an enable signal. Therefore, it would have been obvious at the time the invention was made to store video from a source into a buffer and only output from the buffer after detecting an enable signal, as taught by Tsubouchi et al., since Tsubouchi et al. states in column 2: lines 49-50 that such a modification would prevent collision between video data streams from multiple sources.

Regarding claim 2, as mentioned previously, Settle et al. produces MPEG-2 transport stream packets (column 4: lines 39-42). As was known in the art at the time of the invention, an MPEG-2 transport stream packet must be 188 bytes long, and consists of a header and a payload. If the header is given an extended length, then the subsequent payload is shortened so that the total length of the header and the payload remains at 188 bytes. As shown in ISO/IEC 1318-1 (MPEG-2), a transport stream includes an "adaptation field length" field that indicates the length, in bytes, of the extended header (pp. 21). Therefore, since Settle et al. is an MPEG-2 transport stream encoder, it is inherent that it includes counters for counting packet header length and total packet length, and a selector to output payload data after a packet header has concluded, to produce valid MPEG-2 transport stream packets.

14. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Settle et al. in view of Tsubouchi et al., and in view of US Patent 5,671,260 A (Yamauchi et al.). Although claim 3 is independent, it discloses a narrower version of every limitation in claims 1 and 2. However, the limitation of claim 3 that the "synchronizing signal" in claim 2 is a "horizontal synchronizing signal for the video data" places the scope of claim 3 outside of the combination of Settle et al. and Tsubouchi et al. Claim 3 additionally specifies that the output video data is in the same packet format as an MPEG-2 Transport Stream packet, and that the memory for storing video data is a FIFO memory.

As discussed at length above, Settle et al. outputs video data as MPEG-2 transport stream packets. In addition, video capture 31 of Tsubouchi et al. contains an output buffer for outputting video to a dedicated bus (column 2: lines 55-57), corresponding with the FIFO memory. However, the enable pulse in Tsubouchi et al. for reading video data from the buffer is not a horizontal synchronization signal.

Yamauchi et al. teaches a digital signal processing apparatus that includes a Phase Locked Loop (PLL) that produces a clock signal locked to the horizontal synchronization signal included with the video input (abstract). Synchronization signal 2 extracts an HSYNC and VSYNC signal from input video signal Sv (column 4: lines 44-50), and control generator 12 extracts the HSYNC signal to produce reference signal Sf1 (column 2: lines 51-56). PLL 13 generates a clock signal Sc1 from reference signal Sf1 (column 4: lines 61-63), and A/D converter 5 samples video signal Sv with respect to the clock signal Sc1, producing digital video Svc (column 5: lines 27-32). Digital

video Svc is stored into memory 6 based on write signal Sw, which is based on the HSYNC and VSYNC signals from the original video (column 5: lines 24-26). Then, the video memory is only written to when video data is transmitted in signal Sv, such as columns 123–824 in a given line in the NTSC standard (column 5: lines 19-24).

Settle et al., in combination with Tsubouchi et al., disclose the claimed invention except for digitizing video according to a horizontal synchronization signal. Yamauchi et al. teaches that it was known to sample video based on a horizontal synchronization signal, as set forth in column 5: lines 6-39. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to synchronize a video transcoder to HSYNC as taught by Yamauchi et al., since Yamauchi et al. states in column 8: lines 1-4 that such a modification would ensure that only relevant video data is encoded and not non-video data transmitted in a horizontal blanking interval, regardless of the variability of this interval.

Regarding the "data valid signal" of claim 4, in Yamauchi et al., video memory write signal Sw is only enabled during the period in a particular line in a video when converted video signal Svc corresponds to effective video data (column 5: lines 17-26). Then, only valid video data is transmitted.

Regarding the memory reset in claim 5, for each given line in an NTSC format, writing signal Sw controls a memory to not read data for the first 122 cycles of clock Sc1 produced from the horizontal synchronization signal, then to write data for the next 720

clock cycles, and to release data, thus clearing and resetting the memory for the next line, for the last 16 clock cycles (column 8: lines 1-15).

Yamauchi discloses the claimed invention except for producing a data valid signal based on a horizontal synchronization signal from a memory write controller instead of a packet header length counter. However, the "data valid signal" in claims 4 and 5 is considered equivalent under the Doctrine of Equivalents to the "writing signal" in Yamauchi et al., since in both the present invention and in Yamauchi et al., the signal performs the same function (controlling a memory storing a video signal), in substantially the same way (in response to a horizontal synchronization signal), to produce substantially the same result (outputting only valid data not in the horizontal blanking interval). See *Graver Tank & Mfg. Co. v. Linde Air Products*, 339 U.S. 605, 85 USPQ 328 (1950).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David N. Werner whose telephone number is (571) 272-9662. The examiner can normally be reached on Monday-Friday from 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571) 272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DNW